Amendments to the Claims:

Re-write the claims as set forth below. This listing of claims will replace all prior versions and listings, of claims in the application:

Listing of Claims:

1. (original) A method for passing clear DVD program streams from a CPU (central processing unit) to an MPEG-2 decoder, comprising the steps of:

reading, via a CPU, DVD data from a DVD drive across a PCI (peripheral component interconnect) bus;

decrypting the DVD data in the CPU and creating packet data;

sending the packet data to a FIFO (first in first out) element via a memory bus;

forwarding the packet data from the FIFO element, via a transport bus, to an MPEG-2 decoder.

2. (original) The method according to claim 1, wherein the FIFO element generates a refill request interrupt when the FIFO element reaches a predetermined "almost empty" state.

3. (original) The method according to claim 2, wherein CPU forwards further packet data to the FIFO element when the CPU detects the refill request interrupt.

4. (original) The method according to claim 1, wherein the method further includes clocking the data out of the FIFO element with a free running clock.

5. (original) The method according to claim 4, wherein the packet data is clocked out of the FIFO element in a range of 10Mb/sec to 60Mb/sec.

6. (original) A method for passing clear DVD program streams from a CPU (central processing unit) to an MPEG type decoder, comprising the steps of:

decrypting the DVD data in the CPU and creating packet data;

sending the packet data to a buffer via a memory bus;

forwarding the packet data from the buffer, via a transport bus, to an MPEG type decoder.

7. (original) The method according to claim 6, wherein the MPEG type decoder is an MPEG-2 decoder.

8. (original) The method according to claim 6, wherein the buffer is a FIFO (first in first out) element.

9. (original) The method according to claim 8, wherein the FIFO element generates a refill request interrupt when the FIFO element reaches a predetermined "almost empty" state.

10. (original) The method according to claim 9, wherein CPU forwards further packet data to the FIFO element when the CPU detects the refill request interrupt.

11. (original) The method according to claim 6, wherein the method further includes clocking the data out of the FIFO element with a free running clock.

12. (original) The method according to claim 11, wherein the packet data is clocked out of the FIFO element in a range of 10Mb/sec to 60Mb/sec.

13. (original) A system for passing clear DVD program streams from a CPU (central processing unit) to a decoder, comprising:

a CPU connected to a first bus interface;

system memory connected to the first bus interface via a memory bus;

a second bus interface connected to the first bus interface via a PCI (peripheral component interconnect) bus;

a DVD data source connected to the second bus interface; and

a packet data decoder connected to the memory bus via a buffer;

wherein the CPU reads DVD data from the DVD data source across the PCI bus, decrypts the DVD data and creating packet data, sends the packet data to the buffer via the memory bus, and wherein the decoder receives the packet data, via the transport bus, from the buffer.

14. (original) The system according to claim 13, wherein the buffer is a FIFO (first in first out) element.

15. (original) The system according to claim 14, wherein the FIFO element generates a refill request interrupt when the FIFO element reaches a predetermined "almost empty" state.

16. (original) The system according to claim 15, wherein CPU forwards further packet data to the FIFO element when the CPU detects the refill request interrupt.

17. (original) The system according to claim 13, wherein the system further includes a free running clock connected to the buffer for clocking the packet data out of the buffer.

18. (original) The system according to claim 17, wherein the packet data is clocked out of the buffer in a range of 10Mb/sec to 60Mb/sec.

19. (currently amended) A set-top box that passes clear DVD program streams from a CPU (central processing unit) to an MPEG type decoder, comprising:

a CPU connected to a first bus interface;

system memory connected to the first bus interface via a memory bus;

a second bus interface connected to the first bus interface via a PCI (peripheral component interconnect) bus;

a DVD data source connected to the second bus interface; and

an MPEG type decoder connected to the memory bus via a buffer;

wherein the CPU reads DVD data from the DVD data source across the PCI bus, decrypts the DVD data and [[creats]] <u>creates</u> packet data, sends the packet data to the buffer via the memory bus, and wherein the MPEG type decoder receives the packet data, via the transport bus, from the buffer.

20. (original) The set-top box according to claim 19, wherein the buffer is a FIFO (first in first out) element.

21. (original) The set-top according to claim 20, wherein the FIFO element generates a refill request interrupt when the FIFO element reaches a predetermined "almost empty" state.

22. (original) The set-top according to claim 21, wherein CPU forwards further packet data to the FIFO element when the CPU detects the refill request interrupt.

23. (original) The set-top according to claim 19, wherein the system further includes a free running clock connected to the buffer for clocking the packet data out of the buffer.

24. (original) The set-top according to claim 23, wherein the packet data is clocked out of the buffer in a range of 10Mb/sec to 60Mb/sec.

25. (original) The set-top according to claim 19, wherein the MPEG type decoder is an MPEG-2 decoder.